Freescale Semiconductor
User's Guide

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MPC8349E-mITX-GP Reference Design Platform User's Guide

The MPC8349E-mITX-GP reference design platform is a system featuring the powerful PowerQUICC™ II Pro processor, which includes a built-in security accelerator. This low-cost, high-performance system solution consists of a printed circuit board (PCB) assembly known as the MPC8349E-mITX-GP Board, plus a board support package (BSP), distributed in a CD image. This BSP enables fastest possible time-to-market for development or integration of applications including media servers, network attached storage devices, and next-generation small office home office/small medium business gateways.

Section 1, "MPC8349E-mITX-GP Board," describes the board in terms of its hardware: the features, specifications, block diagram, connectors, interface specification, and hardware straps.

Section 2, "Getting Started," describes the board settings and physical connections needed to boot the MPC8349E-mITX-GP board.

Section 3, "MPC8349E-mITX-GP Software," describes the software that is shipped with the platform.

Use this manual in conjunction with the following documents:

- *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual* (MPC8349ERM)

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WARNING

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (MPC8349EEC)
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582)

1 MPC8349E-mITX-GP Board

This section presents the features and block diagram, specifications, and mechanical data for the MPC8349E-mITX-GP board.

1.1 Features

This section presents the features, specification, and block diagram of the MPC8349E-mITX-GP board. The features are as follows:

- CPU: Freescale MPC8349E running at 533/266 MHz (CPU/CSB (Coherent System Bus))
- Memory subsystem:
  - 128 MByte unbuffered DIMM SDRAM that is expandable to 1 Gbyte
  - 8 MByte Flash memory (one Macronix™ MX29LV640M Flash memory bankorone ESSI EN29LV640 Flash memory bank)
- Interfaces:
  - 10/100/1000 BaseT Ethernet ports:
    - TSEC1, GMII interface: one 10/100/1000 BaseT RJ-45 with RJ-45 interface using Vitesse™ VSC8201 single port 10/100/1000 BaseT PHY
  - USB 2.0 host and OTG:
    - USB2, ULPI interface: one USB2.0 type mini-AB receptacle connector, with SMSC™ USB3300 Hi-Speed USB host/device/OTG PHY
  - PCI2: 32-bit PCI interface running at up to 66 MHz
    - One 32-bit 3.3 V PCI slot connected to PCI-2
  - ST M24256 Serial EEPROM
  - Dallas™ DS1339 RTC with battery holder
- Board connectors:
  - 2 × 10 ATX power supply connector
  - RS-232 connectors
    - 1 × 9 pin DB9 receptacle
    - JTAG/COP for debugging
  - Form factor: Mini-ITX form factor (170 mm × 170 mm, or 6692 mils × 6692 mils)
- 6-layer Printed Circuit Board (4-layer signals, 2-layer power and ground)

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Figure 1 shows the MPC8349E-mITX-GP board block diagram.

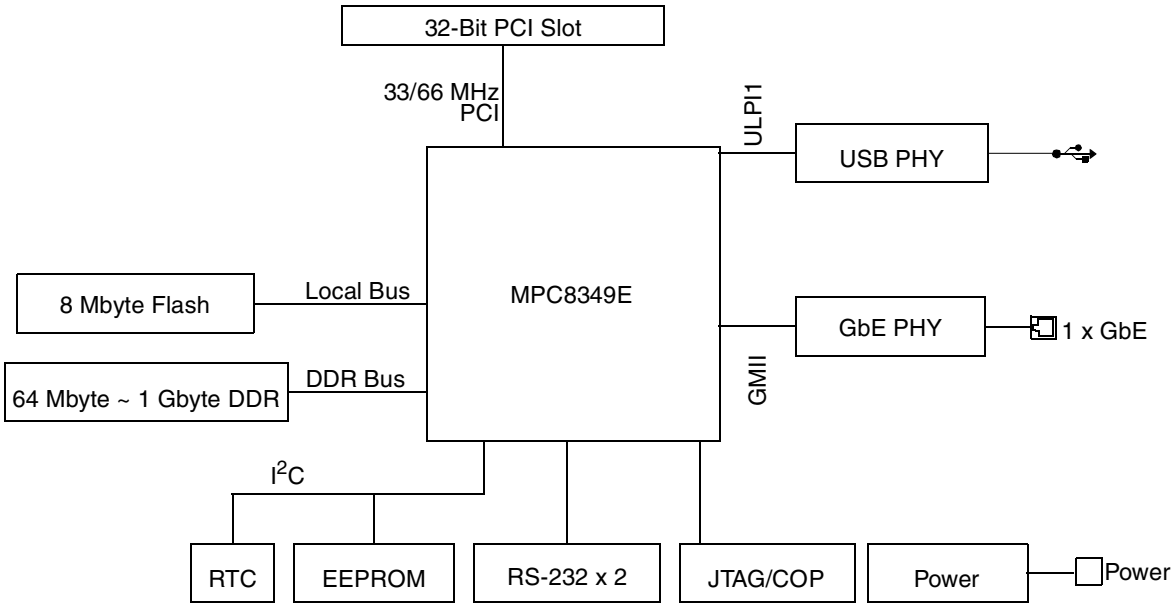

Figure 1. MPC8349E-mITX-GP Board Block Diagram

1.2 Board-Level Functions

The board-level functions discussed in this section are reset, interrupts, and clock distribution.

1.2.1 Reset and Reset Configurations

The MPC8349E-mITX-GP reset module generates a single reset to reset the MPC8349E and other peripherals on the board. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the MPC8349E hardware specification.

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Figure 2 shows the reset circuitry.

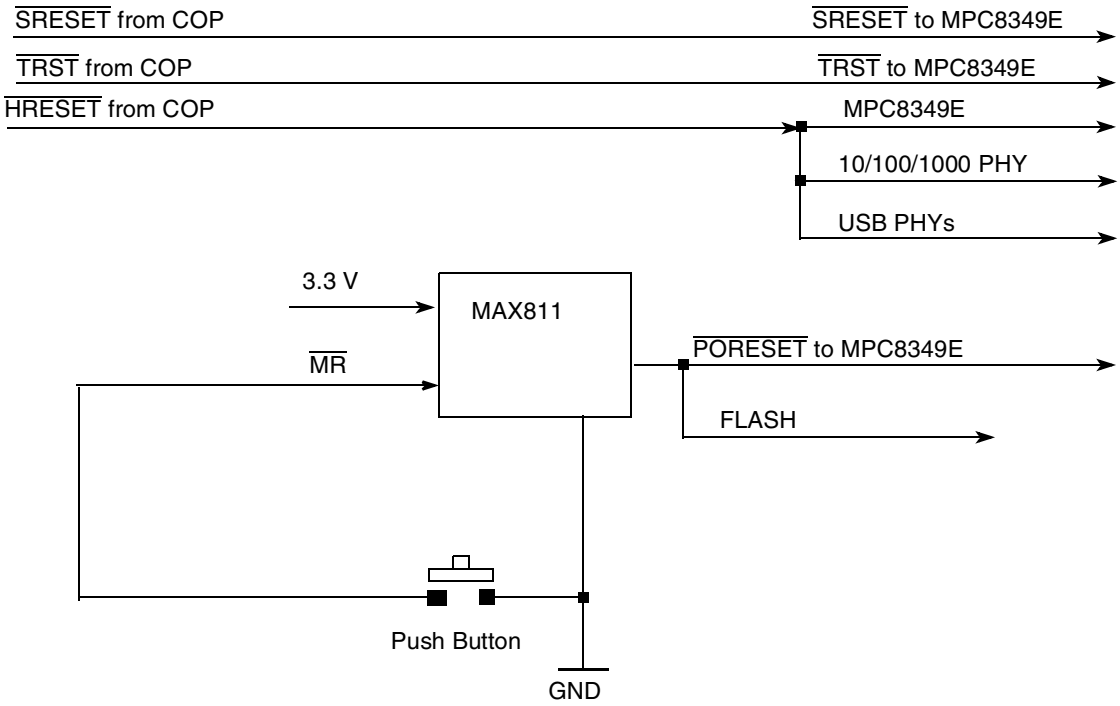

Figure 2. Reset Circuitry of the MPC8349E

- Hard reset is generated either by the COP/JTAG port or the MPC8349E.
- Power-on reset is generated by the Maxim MAX811 device. When MR is deasserted and 3.3 V is ready, the MAX811 internal timeout guarantees a minimum reset active time of 150 ms before PORESET is deasserted. This circuitry guarantees a 150 ms PORESET pulse width after 3.3 V reaches the right voltage level, and this meets the specification of the PORESET input of MPC834x.
- COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The RESET line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low.
- Push button reset interfaces the MR signal with a debounce capability to produce a manual master reset of the processor card.
- Soft reset is generated by the COP/JTAG port. Assertion of SRESET causes the MPC8349E to abort all current internal and external transactions and set most registers to their default values.

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1.2.2 External Interrupts

Figure 3 shows the external interrupt circuitry to the MPC8349E.

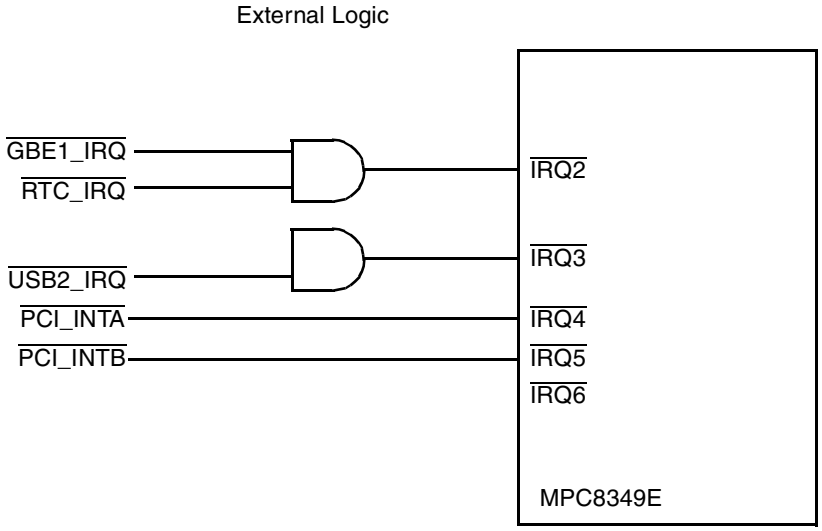

Figure 3. MPC8349E Interrupt Circuitry

Following are descriptions of the interrupt signals shown in Figure 3:

- PHY interrupt ($\overline{\text{GBE1_IRQ}}$) and RTC interrupt ($\overline{\text{RTC_IRQ}}$).The VSC8201 GBE PHY interrupt is ORed with the DS1339 RTC interrupt and connected to $\overline{\text{IRQ2}}$ of the MPC8349E. Therefore, the system software can detect the status of the Ethernet link, the PHY internal status, and the RTC status.
- PCI interrupt ($\overline{\text{PCI_INTA}}$, $\overline{\text{PCI_INTB}}$). The 32-bit PCI slot $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ are connected to the $\overline{\text{IRQ4}}$ and $\overline{\text{IRQ5}}$ of the MPC8349E, respectively.
- USB over current ($\overline{\text{USB2_IRQ}}$). The USB2 power supply has an over current detection circuit and generate an interrupt when the current limit reaches (2A) or a thermal shutdown or under voltage lockout (UVLO) condition occurs. This interrupt pin generates an interrupt to $\overline{\text{IRQ3}}$ of the MPC8349E.

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1.2.3 Clock Distribution

Figure 4 and Table 1 show the clock distribution on the MPC8349E-mITX-GP board.

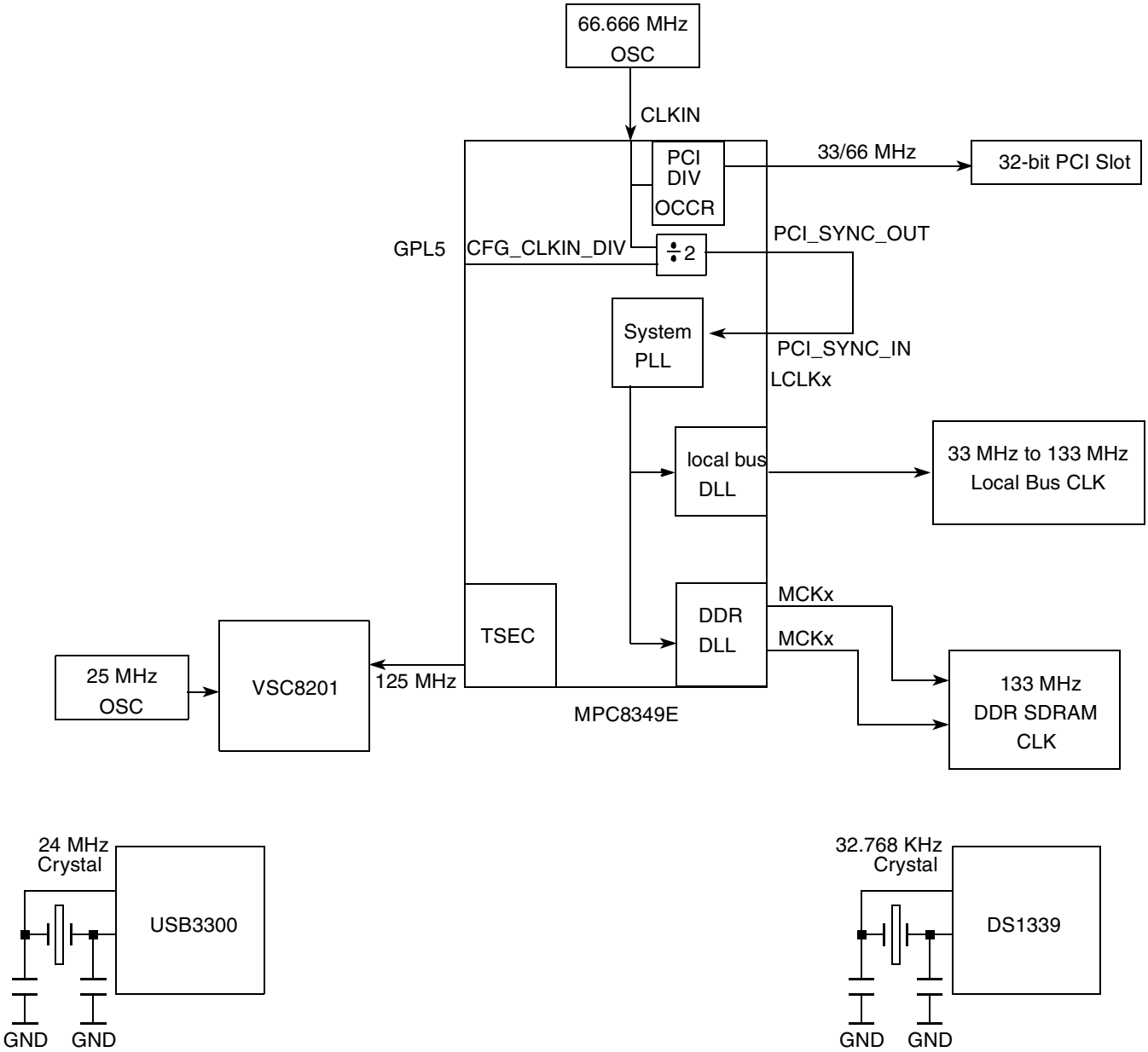

Figure 4. MPC8349E-mITX-GP Clock Scheme

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Table 1. Clock Distribution

Clock Frequency	Module	Generated by	Description
66.666 MHz	MPC8349E CLKIN	66.666 MHz oscillator	The MPC834x uses CLKIN to generate the PCI_SYNC_OUT clock signal, which is fed back on the board through the PCI_SYNC_IN signal to the internal system PLL. From the power-on reset configuration, the CSB clock is generated by the internal PLL and is fed to the e300 core PLL for generating the e300 core clock. The GPL5 (CFG_CLKIN_DIV) configuration input selects whether CLKIN or CLKIN/2 is driven on the PCI_SYNC_OUT signal. The GPL5 is tied to jumper J22.D.
125 MHz	MPC8349E TSEC	VSC8201	For TSEC operation, a 125 MHz clock is provided by the gigabit Ethernet PHY (VSC8201) on the board.
133/166 MHz	DDR SDRAM	MPC8349E	The DDR memory controller is configured to use the 1:1 mode CSB to DDR clock for the DDR interface. The local bus clock uses CCB/n clock, where n is configured from the LCRR register.
25 MHz	GBE PHY (VSC8201)	125 MHz oscillator	The 25 MHz oscillator generates the clock for the VSC8201
33/66 MHz	PCI 32-bit slot	MPC8349E	The PCI module uses the PCI_SYNC_IN as its clock source. The trace of the PCI_SYNC_IN/ PCI_SYNC_OUT signal is synchronized with all the PCI signals of the PCI slots. The trace length of the PCI_SYNC_IN/PCI_SYNC_OUT clock is 2.5 inches from the pin of the PowerQUICC II Pro device to the PCI sockets.
24 MHz	USB PHY2 (USB3300)	24 MHz crystal	
32.768 KHz	RTC (DS1339)	32.768 KHz crystal	

1.2.4 DDR SDRAM Controller

MPC8349E uses DDR SDRAM as the system memory. The DDR interface uses the SSTL2 driver/receiver and 2.5 V power. A Vref 2.5V/2 is needed for all SSTL2 receivers in the DDR interface. For details on DDR timing design and termination, refer to the Freescale application note entitled *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582). The termination scheme uses one series resistor (R_S) from the MPC8349E to the memory and one termination resistor (R_T) attached to the termination rail (V_{TT}). This approach is used in commodity PC motherboard designs.

The MPC8349E reads the DIMM SPD data using the DIMM SCL (clock) and the SDA (data) signals through the I2C2 interface. Figure 5 shows the DDR SDRAM controller connection.

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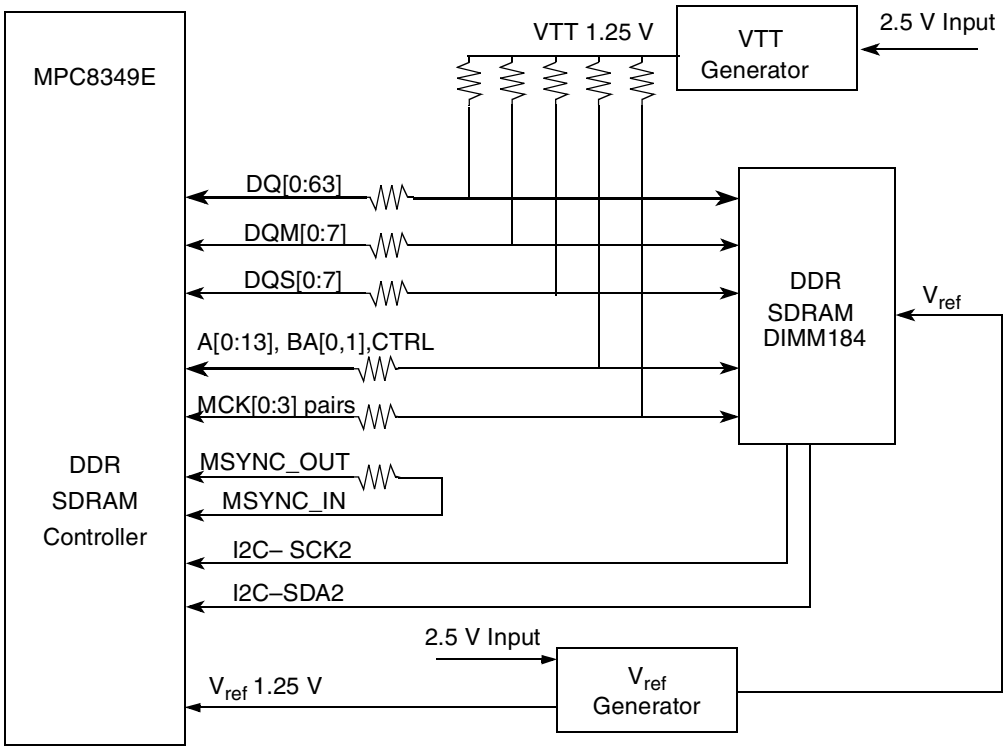

Figure 5. DDR SDRAM Connection

1.2.5 Local Bus Controller

The MPC8349E local bus controller has a 32-bit LAD[0–31] address that consists of data multiplex bus and control signals. The local bus speed is up to 133 MHz. To interface with the standard memory device, an address latch must provide the address signals. The LALE is used as the latching signal. To reduce the load of the high speed 32-bit local bus interface, there is a data buffer for all low-speed devices attached to the memory controller. The on-board single bank 8-Mbyte Flash memory module is connected to the local bus.

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Figure 6 shows the block diagram and connections for the local bus.

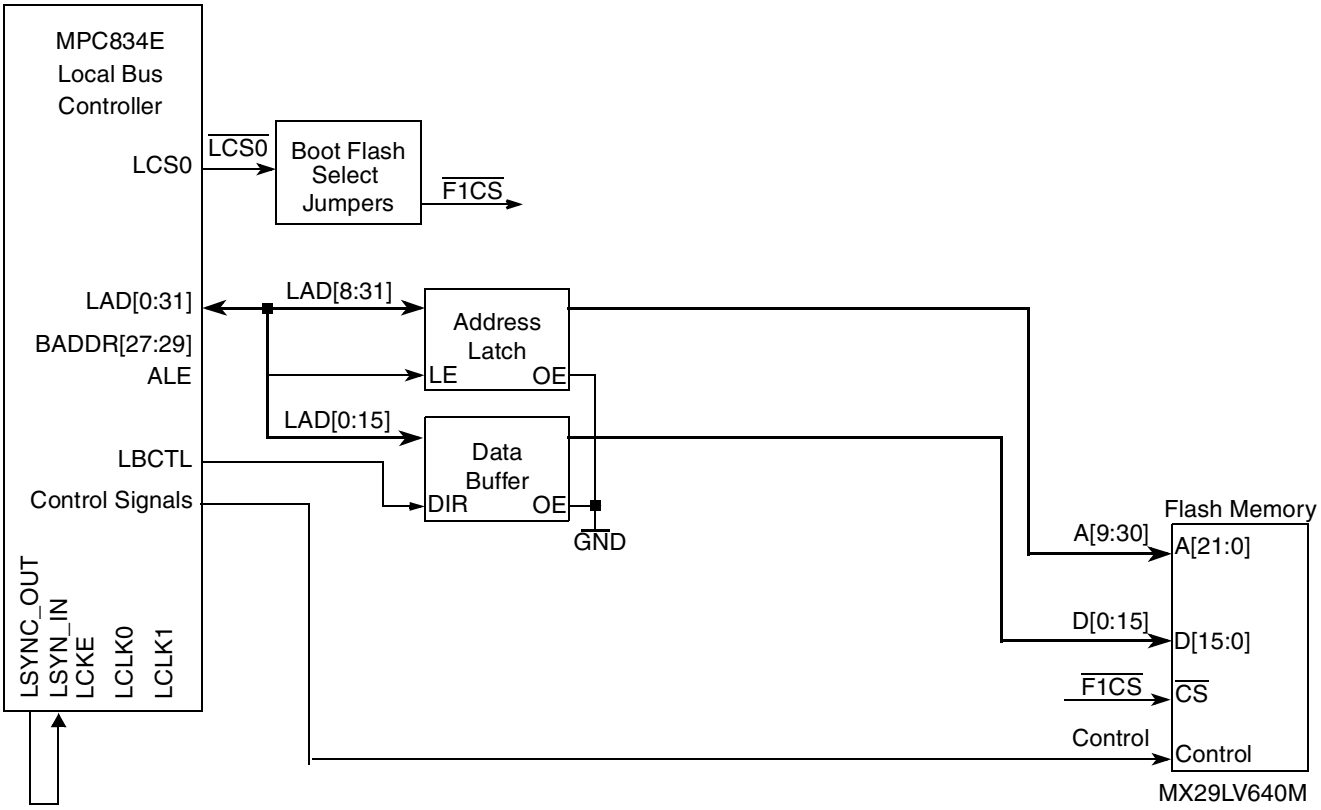

Figure 6. Local Bus Connections

1.2.6 On-Board Flash Memory

Through the general-purpose chip-select machine (GPCM), the MPC8349E-mITX-GP provides a total of 8 Mbyte of 90 ns Flash memory using one chip-select signal. The Flash memory is used with the 16-bit port size.

Table 2. Boot Flash Selection

J22.E	BOOT1	Boot Flash	Backup Flash
Jumper Off	1	Reserved	Reserved
Jumper On	0	U7	U4

The starting address for the Flash bank is 0xFE00_0000 to 0xFE7F_FFFF.

1.2.7 I^2C

The MPC8349E has two I^2C interfaces. On the MPC8349E-mITX-GP board, the MPC8349E acts as I^2C master for both I^2C buses (I2C1 and I2C2). I2C1 is connected to the M24256 serial EEPROM, and I2C2

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is connected to the DDR DIMM module SPD (serial presence detect) EEPROM, the two PCF8574 I^2C expanders, the DS1339 RTC (real time clock).

The M24256 serial EEPROM can be used to store the reset configuration word of the MPC8349E, as well as storing the configuration registers values if boot sequencer of MPC8349E is enabled. If user wants to load the reset configuration word from the I2C1 M24256 EEPROM, the jumper J22 should be set to ABCDEFGH=01011110, with 1=jumper removed and 0=jumper installed. For more details on how to program the reset configuration word value in I^2C EEPROM and the boot sequencer mode, please refer to the MPC8349ERM. The I^2C address of the M24256 EEPROM on I2C1 bus is 0x50.

The DDR SPD EEPROM is connected to the I2C2 of MPC8349E. The bootload program optionally reads the SPD EEPROM data to determine the DDR DIMM physical structure (e.g. number of rows and columns), the DDR timings (e.g. CAS latency, re-fresh timing), and setup the configuration registers of the MPC8349E DDR memory controller. The I^2C address of the DDR SPD EEPROM on I2C2 bus is 0x51.

There are two PCF8574A I^2C I/O expander on the MPC8349E-mITX-GP board to provide general purpose I/O expansion via the I2C2 interface. The first PCF8574A (U8) has I2C2 address 0x38 and it is able to control the Green LED (D1) and Yellow LED (D2), set the VSC8201 to powerdown mode. The bit definition of this PCF8574A (U8) is defined as in Table 3.

Table 3. PCF8574A (U8) Bit Descriptions

PCF8574A (U8) Bit[0..7]	Name	Read/Write	Description
0	LED0	Write only, read returns 1	LED0 control 0: LED is on 1: LED is off
1	LED1	Write only, read returns 1	LED1 control 0: LED is on 1: LED is off
2	VSC8201_PWN	Write only, read returns 1	VSC8201 power down control 0: VSC8201 PHY is powerdown 1: VSC8201 PHY in normal mode
3	Reserved	Write only, read returns 1	Reserved
4	LCD_EN	Write only, read returns 1	Reserved
5	Not used	—	—
6	Not used	—	—
7	Not used	—	—

The second PCF8574A (U10) has I2C2 address 0x39 and it is able to detect the board revision number, the PCI M66EN signal level and detect which Flash is currently used to boot. The bit definition of this PCF8574A (U10) is defined as in Table 4.

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Table 4. PCF8574A (U10) Bit Descriptions

PCF8574A (U10) bit[0..7]	Name	Read/Write	Description
0	REV1	Read only, write has no effect	Board revision number REV[0:1] definition 00: revision 0.0 01: revision 0.1 10: revision 1.0 11: reserved
1	REV0		
2	Reserved	Read only, write has no effect	Reserved for future use
3	Reserved	Read only, write has no effect	Reserved
4	MPCI_CLKRUN	Read/Write	Reserved
5	PCI_M66EN	Read only, write has no effect	PCI M66EN Signal 0: PCI M66EN signal is low, indicates the PCI cards on PCI slot is not 66 MHz capable 1: PCI M66EN signal is high, indicates the PCI cards on PCI slot is 66 MHz capable
6	BOOT0	Read only, write has no effect	Used to determine which Flash is used for boot Flash 0: Reserved 1: Flash 1 (U7) is the boot Flash
7	Not used	—	—

The DS1339 RTC is connected to I^2C with address 0x68. The software running on PowerPC core can read or write to the RTC through the I2C2 interface.

1.2.8 10/100/1000 BaseT Interface

On the MPC8349E-mITX-GP board, GMII mode is used on TSEC1 , which is connected to the on-board 10/100/1000 PHY (VSC8201). The TSEC I/O voltage is set to 3.3 V. The GMII (1000 BaseT) is a source synchronous bus. For a transmit bus connection, it is synchronous to GTX_CLK from the TSEC module. The receive bus connection is synchronous to RX_CLK generated from the PHY device. When the speed is 10/100 BaseT (MII), both transmit and receive clocks are generated by the VSC8201 PHY device. The MPC8349E MII management interface is connected to the VSC8201 only. Figure 7 shows the connection between the MPC8349E TSEC1 to the VSC8201.

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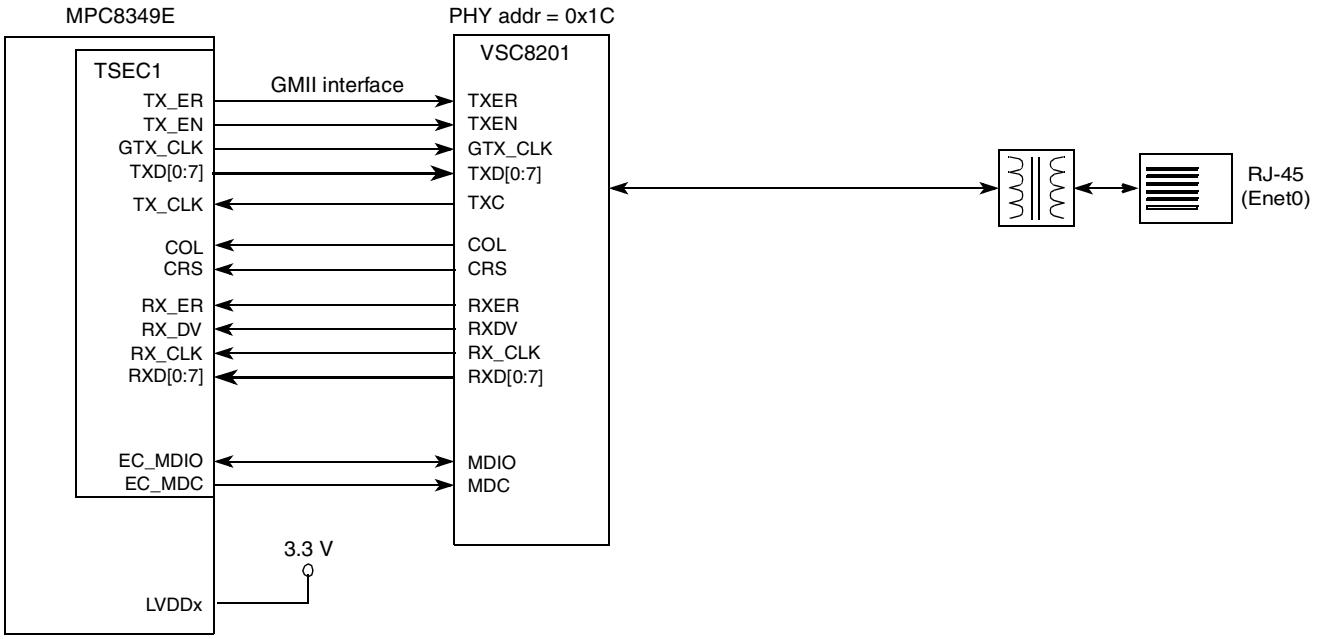

Figure 7. GMII Interface Connection for 10/100/1000 BaseT Ethernet

1.2.9 RS-232 Port

Figure 8 illustrates the serial port connection using a MAX3232 3.3 V RS-232 driver to interface with a 9-pin D type female connector. This serial connection runs at up to 115.2 Kbps.

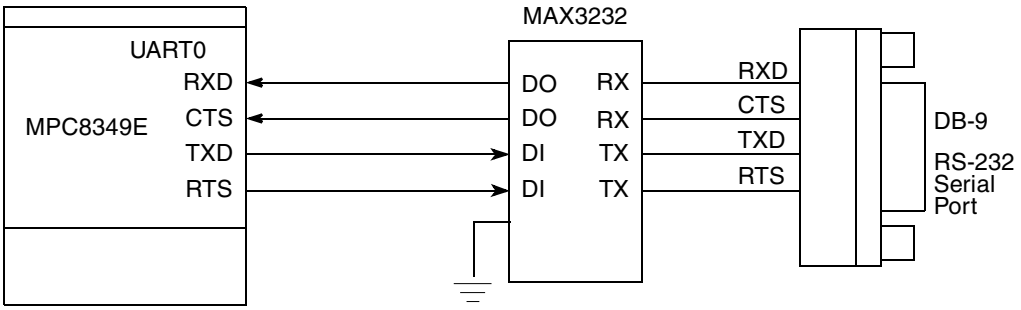

Figure 8. UART Debug Port Connection

1.2.10 USB 2.0 Interface

The MPC8349E has two internal USB modules (USB0 and USB1), a multi-port host (MPH) module, and a dual-role (DR) module. On the MPC8349E-mITX-GP board, USB1 connects to USB PHY (USB3300) through the 8-bit UTMI low pin count interface (ULPI). The USB3300 PHY connects to a USB Mini-AB type receptacle connector that serves as a host/device/OTG USB interface. Table 5 shows the USB0 and USB1 configuration. Note that OTG software support is subject to Linux kernel support.

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Table 5. USB Port 0 and Port 1 Configurations

Port	Interface Type	USB PHY	Operating Mode		Connector Type
USB Port 1	ULPI	USB3300	DR Host/Device/OTG		1 x Type Mini-AB Receptacle

Figure 9 shows the connection of USB port 0 and port 1.

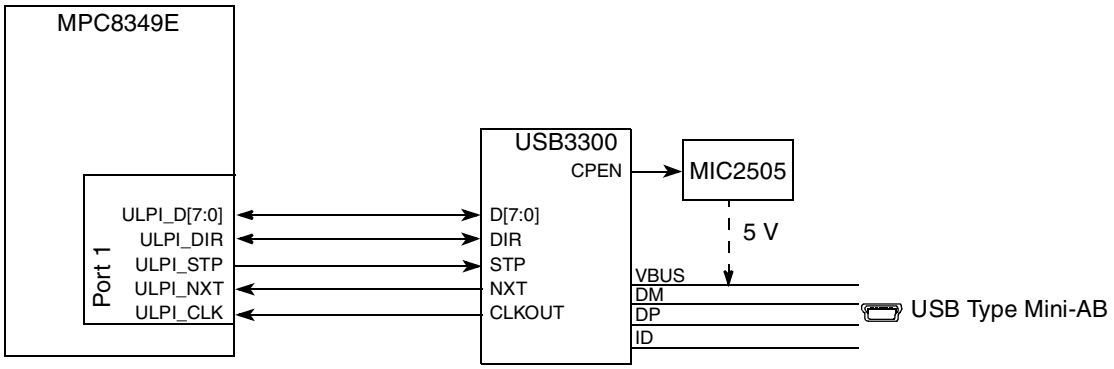

Figure 9. USB Port 0 and Port 1 Connections

1.2.11 PCI Subsystem

The MPC8349E has two PCI interfaces (PCI1 and PCI2). PCI1 interface is not used. PCI2 connects to a 32-bit 3.3 V PCI slot.

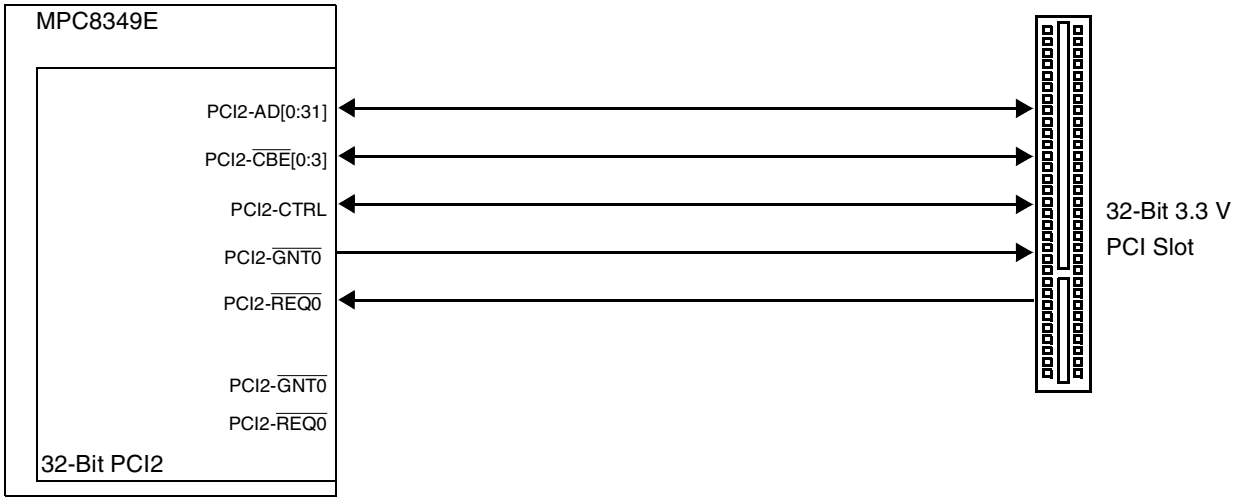

Figure 10. PCI Subsystem

1.2.12 COP/JTAG Port

The common on-chip processor (COP) is part of the MPC8349E JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the

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Ethernet port, USB port, parallel port, RS-232, and so on. A typical setup using a USB port emulator is shown in Figure 11.

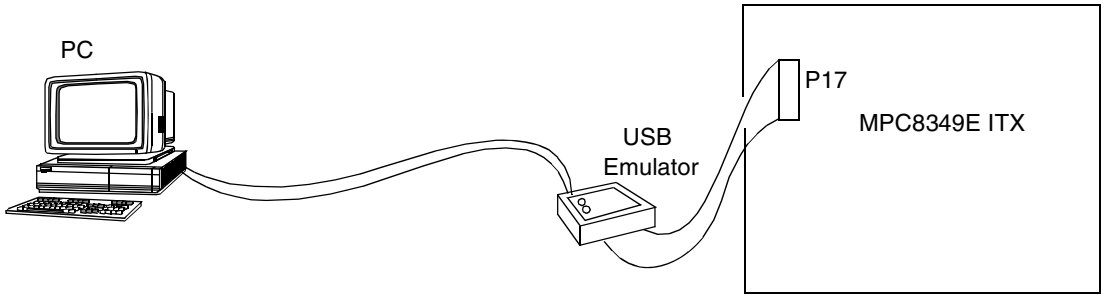

Figure 11. Connecting the MPC8349E-mITX-GP Board to A Parallel Emulator

The 16-pin generic header connector carries the COP/JTAG signals and the additional signals for system debugging. The pinout of this connector is shown in Figure 12.

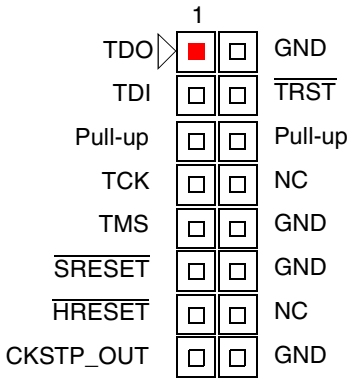

Figure 12. MPC8349E-mITX-GP Board COP Connector

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1.3 MPC8349E-mITX-GP Assembly

The MPC8349E-mITX-GP board PCB top view is shown in Figure 13, with the references of LEDs, jumpers, headers, and switches.

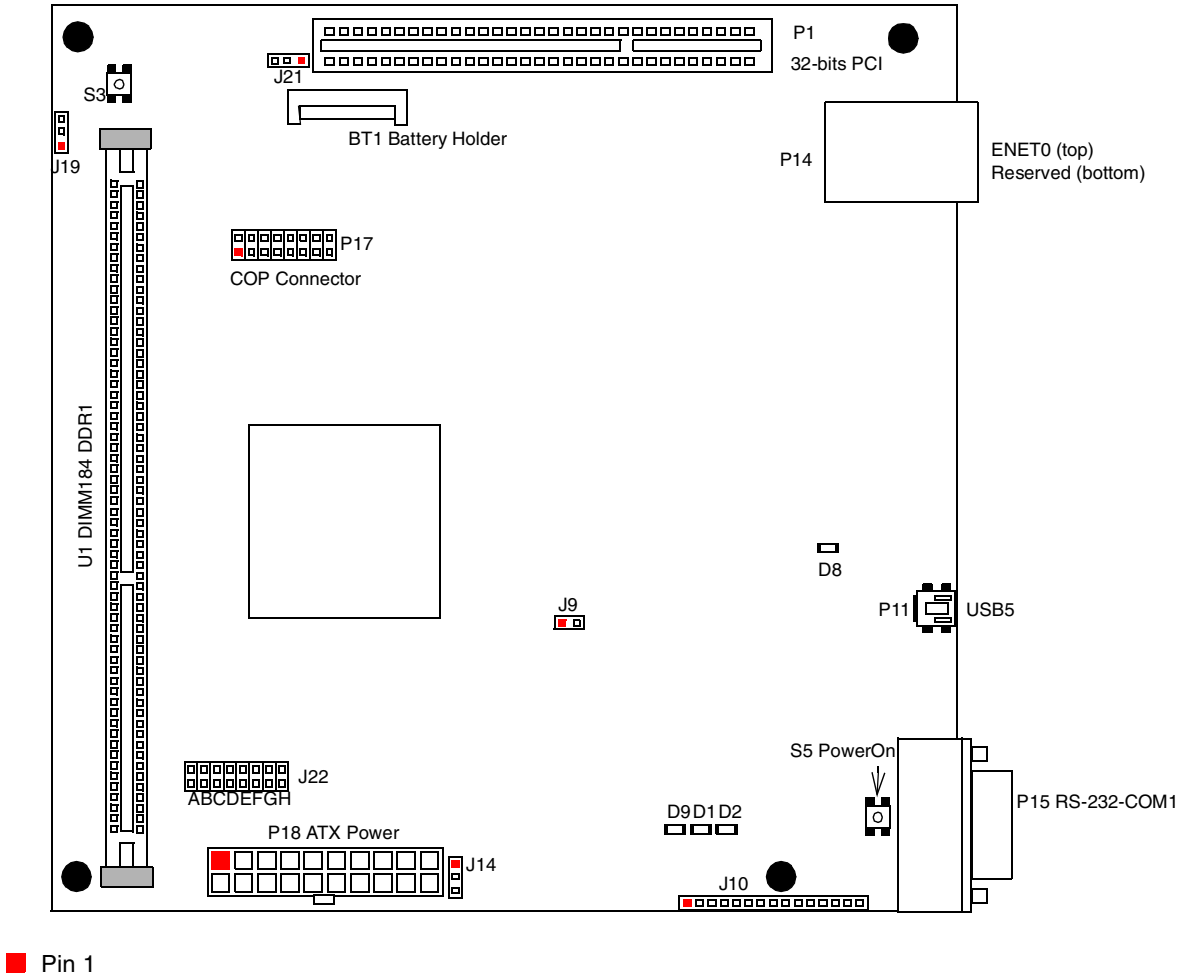

Figure 13. MPC8349E-mITX-GP Top View

1.4 Connectors

This section describes the MPC8349E-mITX-GP connectors and their pin assignments.

1.4.1 Case Connector

The case connector (J10) connects to the case power switch, power LED, reset switch.

- PWR_SW can connect to the 2-pin power push button on the front panel.
- PWR_LED lights when the system is turned ON.
- RST_SW can connect to the 2-pin reset push button on the front panel.

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Table 6 lists the pin assignments of the case connector.

Table 6. Case Connector J10 Pin Assignments

Pin	Signal
1	Power LED K
2	Power LED A
3	Power LED A
4	GND
5	Power On
6	GND
7	RESET
8–15	Reserved

1.4.2 COP Connector

The COP connector (P17) allows the user to connect a COP/JTAG-based debugger to the MPC8349E-mITX-GP board for debugging. Table 7 lists the pin assignments of the COP connector.

Table 7. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	TDO	2	GND
3	TDI	4	$\overline{\text{TRST}}$
5	$\overline{\text{QREQ}}$	6	VDD_SENSE
7	TCK	8	$\overline{\text{CHKSTOP_IN}}$
9	TMS	10	NC
11	$\overline{\text{SRESET}}$	12	NC
13	$\overline{\text{HRESET}}$	14	GND

1.4.3 PCI Slot

The MPC8349E-mITX-GP board has one 32-bit 3.3 V PCI expansion slot (P1) for an expansion card.

WARNING

Only the 3.3 V PCI Card is supported. Turn OFF power during insertion and removal of PCI card.

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3.3 V PCI cards can be identified by the key position on the PCI card, as shown in Figure 14.

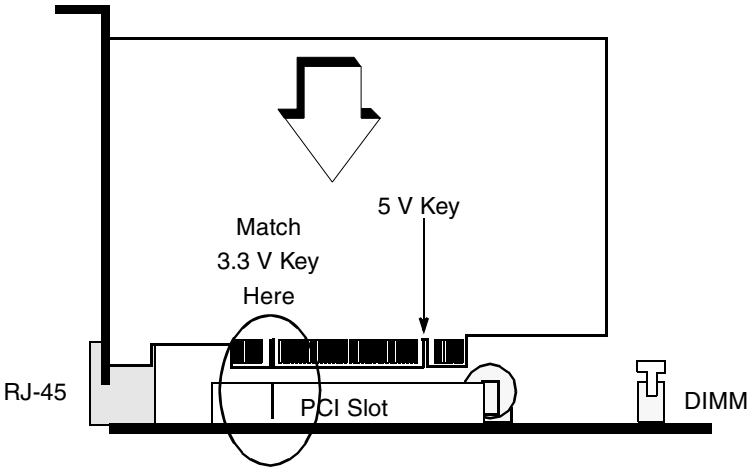

Figure 14. 3.3 V Key on a Typical 3.3 V PCI Card

1.4.4 Fan Connectors

There are two fan connectors on the MPC8349E-mITX-GP board, one for powering a 5 V fan (J9) and the other for powering a 12 V fan (J5). For typical fans, the red wire is always positive (+) and the black wire is always negative (–).

1.4.5 Battery Holder

The MPC8349E-mITX-GP board contains an RTC that requires a battery to maintain the data inside the RTC. The battery holder (BT1) accommodates a CR-2032. Figure 15 shows how to insert a battery.

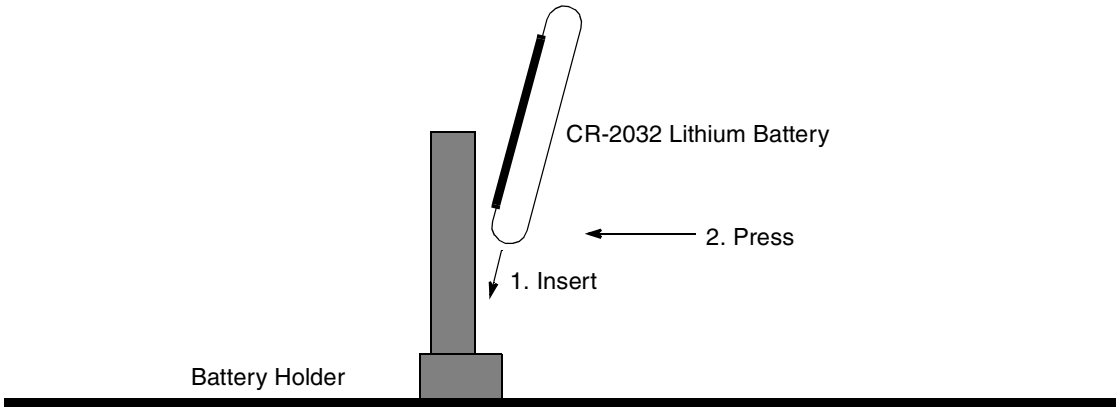

Figure 15. Installation of Battery

1.4.6 Power Connector

P18 is compatible with connectors from ATX power supply, supplying necessary DC power to the MPC8349E-mITX-GP board.

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1.5 Jumpers, Switches, and LED Indicators

This section shows the default settings and descriptions of jumpers, switches, and LED indicators.

1.5.1 Powerup Configuration Jumpers

The powerup configuration jumpers at J22 sets up the system configurations. Figure 16 shows the factory default configuration of J22.

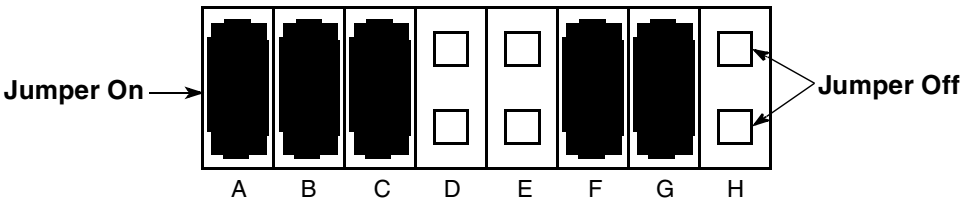

Figure 16. Powerup Configuration Jumpers (J22)

Table 8 describes the position of each jumper.

Table 8. Description of Jumper J22 Positions

Position	Name	Default ON = Jumper Is On OFF = Jumper Is Off	Description
A	LGPL0	ON (0)	000 local bus EEPROM (Default) 001 I^2C EEPROM,PCI_CLK/PCI_SYNC_IN 25–44 MHz 010 I^2C EEPROM,PCI_CLK/PCI_SYNC_IN 25–66.666 MHz 011 Hard-coded option, 66 MHz, 266 MHz, 400 MHz (PCI, CSB, CPU) 100 Hard-coded option, 33 MHz, 266 MHz, 400 MHz 101 Hard-coded option, 33 MHz, 133 MHz, 266 MHz 110 Hard-coded option, 33 MHz, 166 MHz, 333 MHz 111 Hard-coded option, 66 MHz, 266 MHz, 533 MHz Hard-coded option is used in conjunction with JTAG debug
B	LGPL1	ON (0)	
C	LGPL3	ON (0)	
D	LGPL5	OFF (1)	OFF (1): Default CLKIN: PCI_SYNC_OUT = 2:1 PCI_CLK_OUT[0:7] = OCCR (max CLKIN/2). 66 MHz CLKIN is used and 33 MHz PCI2. ON (0): CLKIN: PCI_SYNC_OUT = 1:1, PCI_CLK_OUT[0:7] = CLKIN. 66 MHz CLKIN is used, 66 MHz PCI2.
E	$\overline{\text{BOOT1}}$	OFF(1)	OFF (1): Default MPC8349E fetches the reset vector from Flash 0 (U4). ON (0): Reserved

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Table 8. Description of Jumper J22 Positions

Position	Name	Default ON = Jumper Is On OFF = Jumper Is Off	Description
F	PCI_M66EN	ON (0)	OFF (1): M66EN signal is determined by the card plugged into the PCI slot (PCI 32-bit slot and MiniPCI slot). ON (0): Default M66EN signal is hardwired to 0, which is hard coded to 33 MHz PCI operation.
G	I2C-WP	ON (0)	OFF (1): I^2C EEPROM (U64) is write protected. ON (0): Default I^2C EEPROM (U64) is not write protected.
H	$\overline{\text{F_WP}}$	OFF (1)	OFF (1): Default Flash (U7) are not write protected. ON (0): Flash (U7) are write protected.

Table 9 lists the connectors, jumpers, switches, and LEDs on the MPC8349E-mITX-GP board.

Table 9. Lists of Connectors, Jumpers, Switches, and LEDs

Reference	Description
Connectors	
BT1	Battery holder for RTC
J4	Background Debug Mode (BDM). Header for Flash programming and debug of on-board MC9S08QG8 Microcontroller.
J5	12V fan connector
J9	5 V fan connector
J10	Case connector
P1	32-bit 3.3 V PCI connector
P11	USB MiniAB connector
P14	RJ-45 connectors Enet0 (top). Typically Enet0 is the WAN connector. See Figure 7.
P15	COM1 serial port terminal connector (RS-232)
P17	14 pins COP/JTAG connector
P18	ATX Power connector
U1	DIMM184 DDR1 connector
Jumpers	
J14	CPU power control jumper. Selects ATX power supply on/off to be controlled by push button S5 (jumper 2–3 as default) or MCU firmware (jumper 1–2).

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Table 9. Lists of Connectors, Jumpers, Switches, and LEDs (continued)

Reference	Description
J19	CPU Power-on reset source jumper. CPU Power-On Reset can be controlled by a hardware MAX811 reset chip (jumper 2–3 as default).
J21	Real time clock selector. CPU real time clock interrupt request can be selected from DS1339 real time clock, [jumper 2–3]. Default is not selected.
J22	Reset configuration word source selection jumpers
Switches	
S3	System reset button. Resets the MPC8349E-mITX-GP board.
S5	Power-on push button. Powers up the MPC8349E-mITX-GP board.
LEDs	
D1/D2	SW0 and SW1. Controlled by the I2C expander connected to the MPC8349E
D8	USB port power indicator LED. Lights when power is enabled on USB (D8).
D9	3.3 V Active. On means 3.3 V power is good.

1.6 MPC8349E-mITX-GP Board Configuration

This section describes the operational mode and configuration options of the MPC8349-mITX-GP board.

1.6.1 Flash Memory

The Flash memory bank is MX29LV640MTTC-90 top boot Flash memory devices. Each Flash memory bank has 135 sectors. The first 127 sectors, SA[0–126], are 64 Kbyte, and the last 8 sectors, SA[127–134], are 8 Kbyte. These last 8 sectors can be write-protected to prevent accidental erasure of the sector content for applications that may choose to use this protection feature. Table 10 shows the jumper settings to write-protect sectors SA[127–134] of Flash memory.

Table 10. Flash Memory Write Protect of SA[127–134]

J22.H	Description
Jumper Off	Flash (U7) top sectors are not write protected ($\overline{WP}$ not asserted).
Jumper On	Flash (U7) top sectors are write protected ($\overline{WP}$ asserted).

1.6.2 EEPROM

An on-board serial EEPROM allows storage of miscellaneous board-related data. The EEPROM can be write-protected by S2.SW3, as shown in Table 11.

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Table 11. EEPROM Write Protect

J22.G	Description
Jumper Off	Serial EEPROM is write protected ($\overline{WC}$ not asserted).
Jumper On	Serial EEPROM is not write protected ($\overline{WC}$ asserted).

1.6.3 PCI Operating Frequency

An M66EN input pin determines the AC timing of the PCI interface. On the MPC8349E-mITX-GP board, the state of this signal can be driven to 0 by the J22 jumper to select 33 MHz AC timing. If J22.F is not driven to 0, the M66EN signal level is determined by the PCI agent card connected to PCI slot P1. If a 33 MHz only card is inserted, the M66EN signal is driven to 0 by the PCI agent card according to the PCI specification, or it is driven to 1 if it can perform at 66 MHz. See Table 12.

Table 12. M66EN Signal Status Selection

J22.F	Description
Jumper Off	M66EN signal is determined by the card plugged into the PCI slot.
Jumper On	M66EN signal is hardwired to 0, which is hard coded to 33 MHz PCI operation.

1.6.4 Reset Configuration Word

The reset configuration word (RCW) controls the clock ratios and other basic device functions such as PCI host or agent mode, boot location, TSEC modes, and endian mode. The reset configuration word is divided into reset configuration word lower (RCWL) and reset configuration word higher (RCWH) and is loaded from the local bus during the power-on or hard reset flow. The default RCW low bit setting is 0x0404_0000. The default RCW high bit setting is 0xB460_A000.

The RCW is located at the lowest 64 bytes of the boot Flash memory, which is 0xFE00_0000 if the default memory map is used.

Table 13. Default RCW in Flash Memory

Address				
FE000000:	04040404	04040404	04040404	04040404
FE000010:	00000000	00000000	00000000	00000000
FE000020:	B0B0B0B0	B0B0B0B0	60606060	60606060
FE000030:	A0A0A0A0	A0A0A0A0	00000000	00000000

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The RCW definitions are shown in Figure 17 and Figure 18.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	LBIUCM	DDRCM	—		SPMF				—	COREPLL						

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	—															

Figure 17. Reset Configuration Word Low (RCWL) Bit Settings

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	PCIHOST	PCI64	PCI1ABR	PCI2ABR	COREDIS	BMS	BOOTSEQ		SWEN	ROMLOC			—			

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	TSEC1M		TSEC2M		—								TLE	LALE	LDP	—

Figure 18. Reset Configuration Word High (RCWH) Bit Settings

Table 14. RCWL Bit Descriptions

Bits	Name	Meaning	Description	
0	LBIUCM	Local bus memory controller clock mode	Local Bus Controller Clock: CSB_CLK	
			0: Default	ratio 1:1
			1:	ratio 2:1
1	DDRCM	DDR SDRAM memory controller clock mode	DDR Controller Clock: CSB_CLK	
			0: Default	ratio 1:1
			1:	ratio 2:1
2–3	—	Reserved	Must be cleared.	
4–7	SPMF[0–3]	System PLL multiplication factor	0000	16:1
			0001	Reserved
			0010	2:1
			0011	3:1
			0100 (default)	4:1
			0101	5:1

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Table 14. RCWL Bit Descriptions (continued)

Bits	Name	Meaning	Description	
4–7	SPMF[0–3]	System PLL multiplication factor	0110	6:1
			0111	7:1
			1000	8:1
			1001	9:1
			1010	10:1
			1011	11:1
			1100	12:1
			1101	13:1
			1110	14:1
			1111	15:1
8	—	Reserved	Must be cleared.	
9–15	COREPLL [0–6]	Value	coreclk: csb_clk	VCO divider
		nn 0000 n	PLL bypassed	PLL bypassed
		00 0001 0	1:1	2
		01 0001 0	1:1	4
		10 0001 0	1:1	8
		11 0001 0	1:1	8
		00 0001 1	1.5:1	2
		01 0001 1	1.5:1	4
		10 0001 1	1.5:1	8
		11 0001 1	1.5:1	8
		00 0010 0: Default	2:1	2
9–15	COREPLL [0–6]	01 0010 0	2:1	4
		10 0010 0	2:1	8
		11 0010 0	2:1	8
		00 0010 1	2.5:1	2
		01 0010 1	2.5:1	4
		10 0010 1	2.5:1	8
		11 0010 1	2.5:1	8
		00 0011 0	3:1	2
		01 0011 0	3:1	4
		10 0011 0	3:1	8
		11 0011 0	3:1	8
16–31	—	Reserved.	Must be cleared.	

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Table 15. Reset Configuration Word High (RCWH) Bit Descriptions

Bits	Name	Meaning	Detailed Description	
0	PCIHOST	PCI host mode	0	PCI agent
			1: Default	PCI host
1	PCI64	PCI 64 bit bus mode	0: Default	32-bit PCI interface
			1	64-bit PCI interface
2	PCI1ARB	PCI1 arbiter	0	PCI1 arbiter disabled
			1: Default	PCI1 arbiter enabled
3	PCI2ARB	PCI2 Arbiter	0	PCI2 arbiter disabled
			1: Default	PCI2 arbiter enabled
3	Reserved	—	Must be cleared	
4	COREDIS	Core disable mode	0: Default	e300 enabled
			1	e300 disabled
5	BMS	Boot memory space	0: Default	0x0000_0000–0x007F_FFFF
			1	0xFF80_0000–0xFFFF_FFFF
6–7	BOOTSEQ	Boot sequencer configuration	00: Default	Boot sequencer is disabled
			01	Boot sequencer load configuration from I^2C
			10	Boot sequencer load configuration from EEPROM
			11	Reserved
8	SWEN	Software watchdog enable	0: Default	Disabled
			1	Enabled
9–11	ROMLOC	Boot ROM interface location	000	DDR SDRAM
			001	PCI1
			010	PCI2
			011, 100	Reserved
			101	Local bus GPCM, 8 bits
			110: Default	Local bus GPCM, 16 bits
			111	Local bus GPCM, 32 bits
12–15	Reserved	—	Must be cleared	
16–17	TSEC1M	TSEC1 Mode	00	RGMII
			01	RTBI
			10: Default	GMII
			10	TBI

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Table 15. Reset Configuration Word High (RCWH) Bit Descriptions (continued)

Bits	Name	Meaning	Detailed Description	
18–19	TSEC2M	TSEC2 Mode	00	RGMII
			01	RTBI
			10: Default	GMII
			10	TBI
20–27	Reserved	—	Must be cleared	
28	TLE	True little endian	0: Default	Big-endian mode
			1	True little endian mode
29	LALE	Local Bus ALE signal timing	0: Default	Normal LALE timing
			1	LALE is negated 1/2 lbiu_controller_clk earlier.
30	LDP	LDP/CKSTP pin mux state after reset	0: Default	LDP[0] and LDP[1] = local data parity.
			1	LDP[0] = CKSTOP_OUT and LDP[1] = CKSTOP_IN.
31	Reserved	—	Must be cleared	

1.6.4.1 Reset Configuration Word SPMF[0–3] and COREPLL[0–6]

CLKIN is the input to the CCB PLL to generate the CCB clock, which provides the platform logic. Table 16 shows the common combinations of CLKIN, CCB, and the core frequency and their respective ratios.

Table 16. Core PLL Ratio

CLKIN	SPMF [0–3]	CCB	CCB clock: CLKIN Ratio	COREPLL [0–6]	Core Frequency	CCB Clock: CLKIN Ratio
66.666 MHz	0101	333 MHz	5:1	00 0010 0	667 MHz	2:1
66.666 MHz	0100	266 MHz	4:1	00 0010 1	667 MHz	2.5:1
66.666 MHz	0011	200 MHz	3:1	00 0010 0	600 MHz	3:1
66.666 MHz	0101	333 MHz	5:1	01 0001 1	500 MHz	1.5:1
66.666 MHz	0100	266 MHz	4:1	00 0010 0	533 MHz	2:1
66.666 MHz	0011	200 MHz	3:1	00 0010 1	500 MHz	2.5:1
66.666 MHz	0101	333 MHz	5:1	00 0001 0	333 MHz	1:1
66.666 MHz	0100	266 MHz	4:1	01 0001 1	400 MHz	1.5:1
66.666 MHz	0011	200 MHz	3:1	01 0010 0	400 MHz	2:1

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1.6.4.2 Example of Changing the RCW Register Using Uboot

Issue the following uboot commands to change from 533/266 to 400/266 (CPU/CCB):

```
cp.b FE000000 100000 40
mw.b 100008 23 8
md 100000
erase FE000000 FE00FFFF
md FE000000
cp.b 100000 FE000000 40
md FE000000
reset
```

To make the changes take effect, power off the system and then power it on. Figure 19 shows the change in bit settings from these uboot commands. There is no change in the SPMF field since 0b0100 is the default value representing the 266 MHz CCB frequency. The COREPLL field is changed from the default value of 0b000_0100 representing 533 MHz to the new value of 0b010_0011 representing 400 MHz core frequency.

	0			3	4			7	8	9						15
Field	—				SPMF				—	COREPLL						
Bit Setting	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	1

Figure 19. Reset Configuration Word Low (RCW) Bit Settings Example

1.6.5 Power Supply

The MPC8349E requires a 3.3 V and 5 V power supply from the ATX power connector for normal operation. The 3.3 V power supply is reduced to 1.2 V and 2.5 V. The 1.2 V power is generated from a switching power supply for a CPU core. The 2.5 V power is generated from an LDO regulator for the DDR controller.

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Figure 20 shows the power supply block diagram.

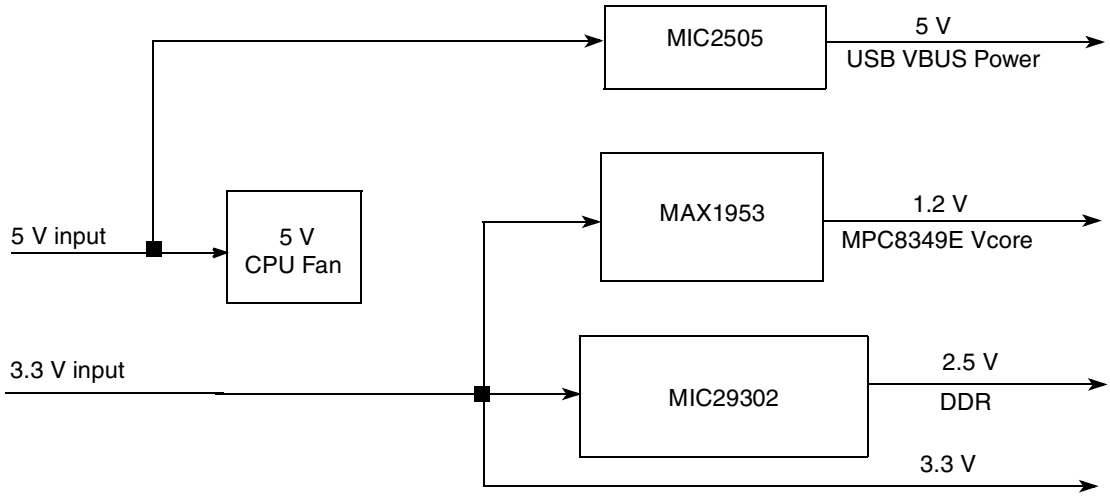

Figure 20. Power Supply Circuitry

The core supply voltage and I/O supply voltages do not have to be applied in any particular order. During the power ramp up, before the power supplies are stable, there may be an interval when the I/O pins are actively driven. After power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most I/O pins are three-stated. To minimize the time I/O pins are actively driven, apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In general, for a dual-supply voltage device, minimize the voltage difference between the V_{core} and $V_{I/O}$ during ramp-up and power-down.

1.6.6 Chip-Select Assignments and Memory Map

Table 17 shows an example memory map on the MPC8349E that is used for u-boot 1.1.3 in the Flash memory.

Table 17. Example Memory Map, Local Access Window, and Chip-Select Assignments

Address Range	Target Interface	Chip-Select Line	Device Name	Port Size (Bits)
0x0000_0000–0x4000_0000	DDR	MCS0/MCS1	DDR SDRAM (256 Mbytes– 1 Gbyte)	64
0x8000_0000–0x9FFF_FFFF	PCI1	Nil	PCI1 memory space (512 Mbyte)	32
0xE200_0000–0xE2FF_FFFF	PCI1	Nil	PCI1 I/O space (16 Mbyte)	32
0xA000_0000–0xBFFF_FFFF	PCI2	Nil	PCI2 memory space (512 Mbyte)	32
0xE300_0000–0xE3FF_FFFF	PCI2	Nil	PCI2 I/O space (16 Mbyte)	32
0xF000_0000–0xF000_FFFF	Local bus	LCS3	Reserved	8
0xF900_0000–0xF91F_FFFF	Local bus	LCS2	Reserved	8
0xF800_0000–0xF801_FFFF	Local bus	LCS1	Reserved	8
0xE000_0000–0xEFFF_FFFF	Internal bus	Nil	IMMR (1 Mbyte)	—

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Table 17. Example Memory Map, Local Access Window, and Chip-Select Assignments (continued)

Address Range	Target Interface	Chip-Select Line	Device Name	Port Size (Bits)
0xFE00_0000–0xFE7F_FFFF	Local bus	LCS0	Boot Flash (8 Mbyte)	16
0xFE80_0000–0xFEFF_FFFF	Local bus	LCS0	Reserved	16

1.7 Specifications

Table 18 lists the specifications of the MPC8349E-mITX-GP board.

Table 18. MPC8349E-mITX-GP Board Specifications

Characteristics	Specifications	
Power requirements:	**Typical**	**Maximum**
	3.3 V DC 3.0 A	6.5 A
	5.0 V DC 300 mA	2.0 A
Communication processor	MPC8349E running @ 533 MHz	
Addressing: Total address range	4 Gbyte (32 address lines)	
Flash memory (local bus)	Up to 16 Mbyte with two chip-selects	
DDR SDRAM	Up to 1 Gbyte DDR SDRAM at DDR333 with optional ECC feature	
Operating temperature	0°C to 70°C (room temperature)	
Storage temperature	–25°C to 85°C	
Relative humidity	5% to 90% (noncondensing)	
PCB dimensions:		
Length	6692 mils	
Width	6692 mils	
Thickness	61.4 mils	

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1.8 Mechanical Data

Figure 21 shows the MPC8349E-mITX-GP dimensions (in mils). The board dimensions are 170 mm × 170 mm (6692 mils × 6692 mils) for integration in a mini-ITX chassis with a small footprint. The locations of the mounting holes are shown in Figure 21.

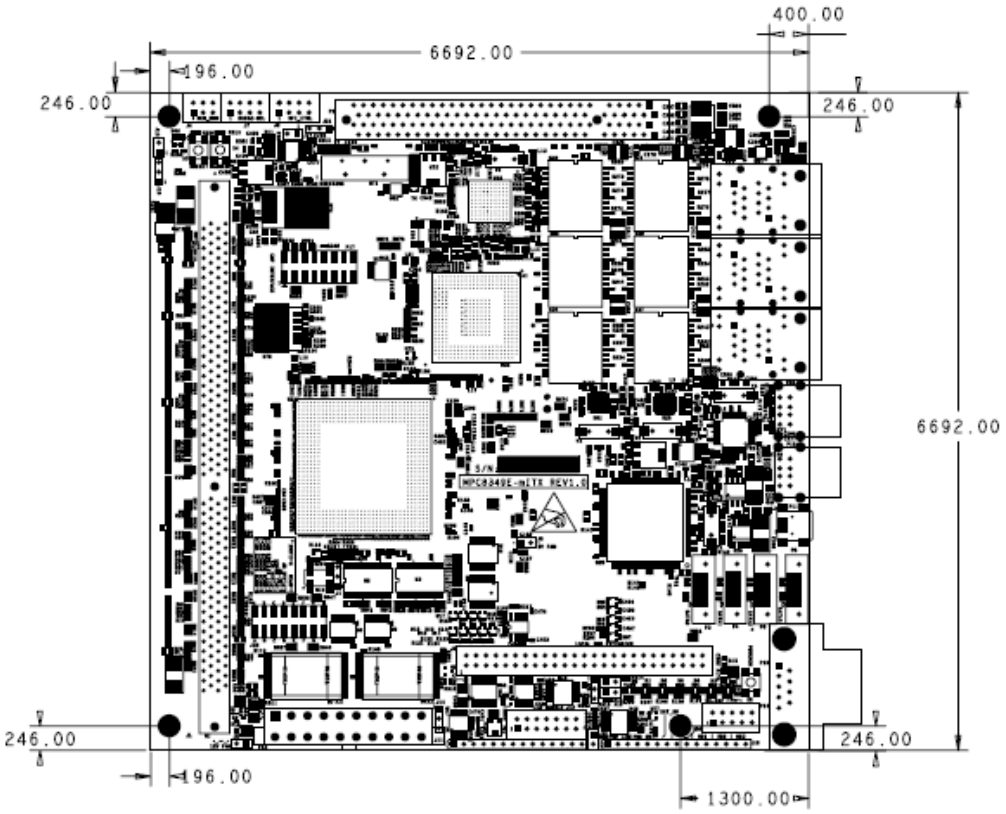

Figure 21. Dimensions of the MPC8349E-mITX-GP Board

2 Getting Started

This section describes how to boot up the MPC8349E-mITX-GP board. The on-board Flash memory has been preloaded with a Flash image from the factory. Before powering up the board, set the on-board jumpers according to the settings listed in Section 2.1, "Board Jumper Settings," install the DDR memory module according to the instructions in Section 2.2, "Install DIMM Module," and then make all the external connections as described in Section 2.3, "External Connections."

CAUTION

Avoid touching areas of integrated circuitry and connectors; static discharge can damage circuits.

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2.1 Board Jumper Settings

Figure 22 shows the top view of the MPC8349E-mITX-GP with pin 1 marked for each reference. Using Figure 22 as a guide, the default jumper settings are given in Table 19 starting at the left-hand top corner of the board and moving around the board in a clockwise manner.

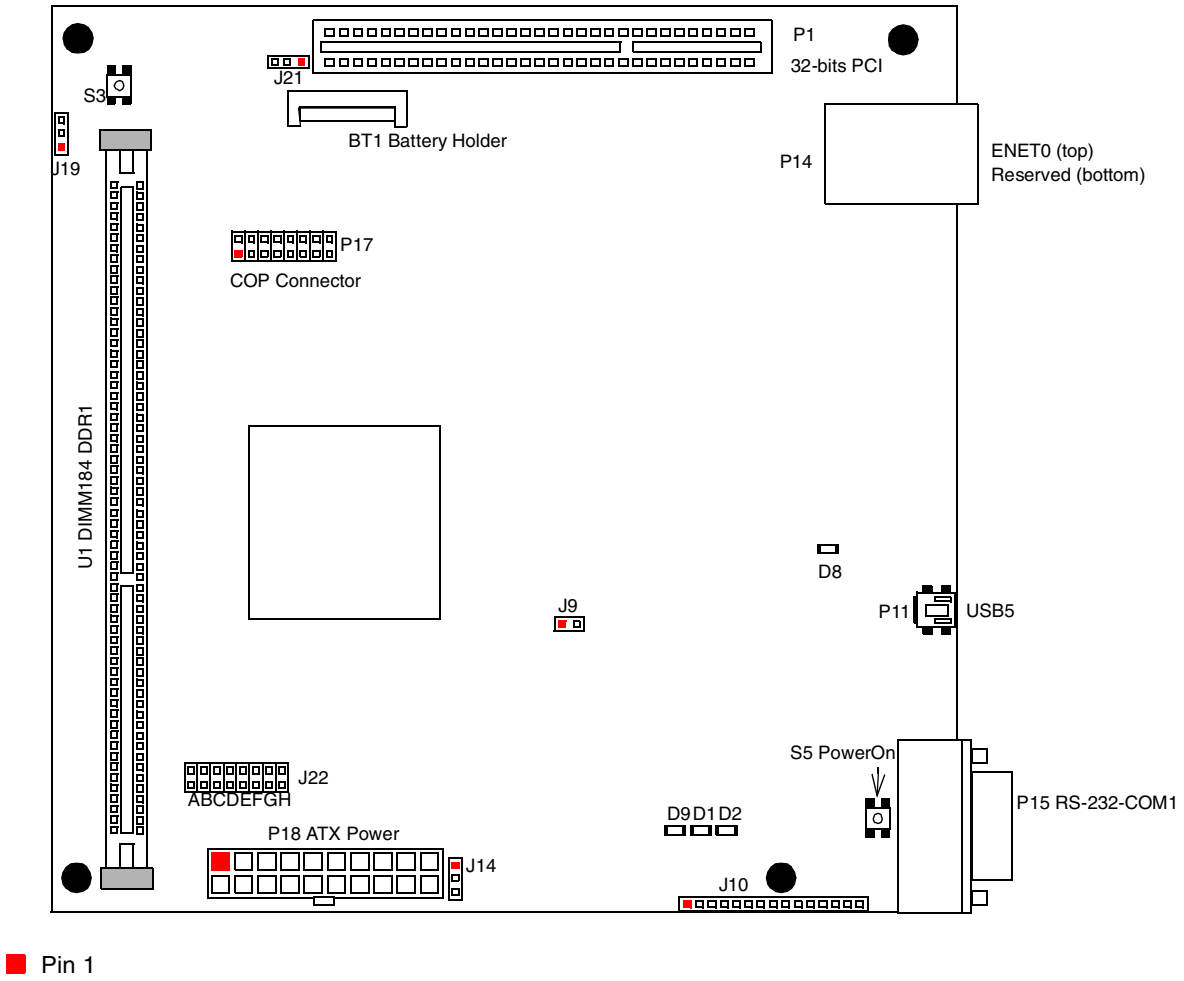

Figure 22. MPC8349E-mITX-GP Top View

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Set the jumpers to their default settings as given in Table 19.

Table 19. Default Jumper Settings

Reference	Default Jumper Setting	√ = Jumper × = No Jumper
J19	2–3	√
J21	not used	×
J14	2–3	√

2.2 Install DIMM Module

A 128-Mbyte DIMM is shipped with the platform. Install this memory module (when the platform is powered down) onto the DIMM connector U1 as shown in Figure 23. This DIMM connector can accommodate 64-MByte to 1-GByte modules. The MPC8349E reads the DDR serial presence detect (SPD) data from the EEPROM on the DIMM module to identify the module type and various SDRAM configurations and timing parameters.

WARNING

Switch the power OFF when installing/removing the DIMM module.

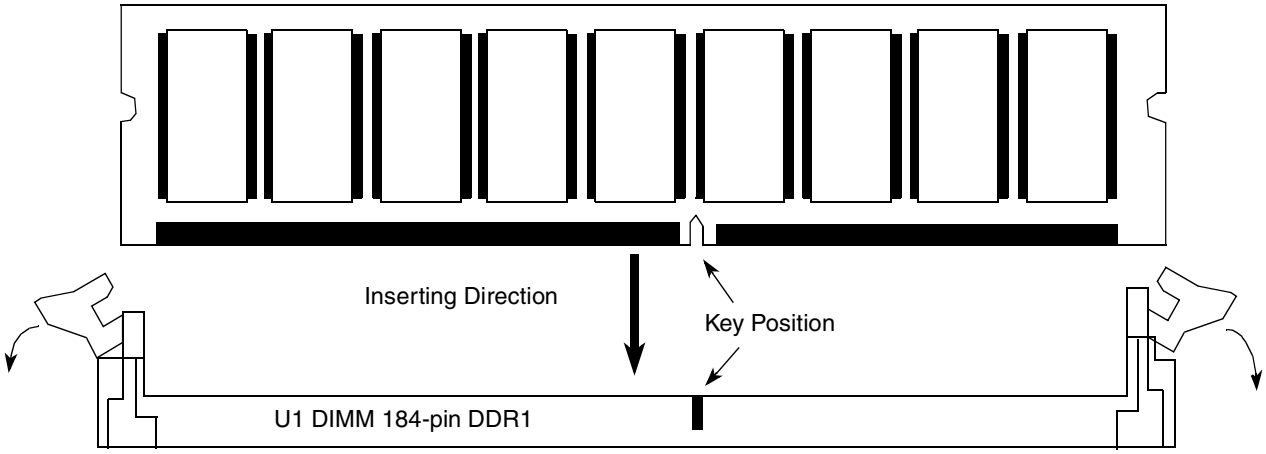

Figure 23. Installing the DDR1 DIMM Module

Both error correcting codes (ECC) and non-ECC DIMM modules are supported. The MPC8349E software reads the module data width field in the SPD EEPROM to determine whether ECC is present and configures the corresponding registers in the internal DDR controller. DDR1 unbuffered DIMM modules with fewer than 12 or greater than 14 row addresses are not supported. DIMM modules with fewer than 8 or greater than 11 column addresses are not supported.

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Table 20. Supported ROW/COLUMN Address Combinations

Row/Column Addresses	Number
ROW	12–14
COLUMN	8–11

2.3 External Connections

Do not turn on power until all cables have been connected and the serial port has been configured as described in Section 2.4, “Serial Port Configuration (PC).”

2.3.1 Cable Connections

Connect the serial port of the -mITX-GP system and the personal computer using RS-232 cable supplied with the system. Then connect the AC adaptor as in shown in Figure 24.

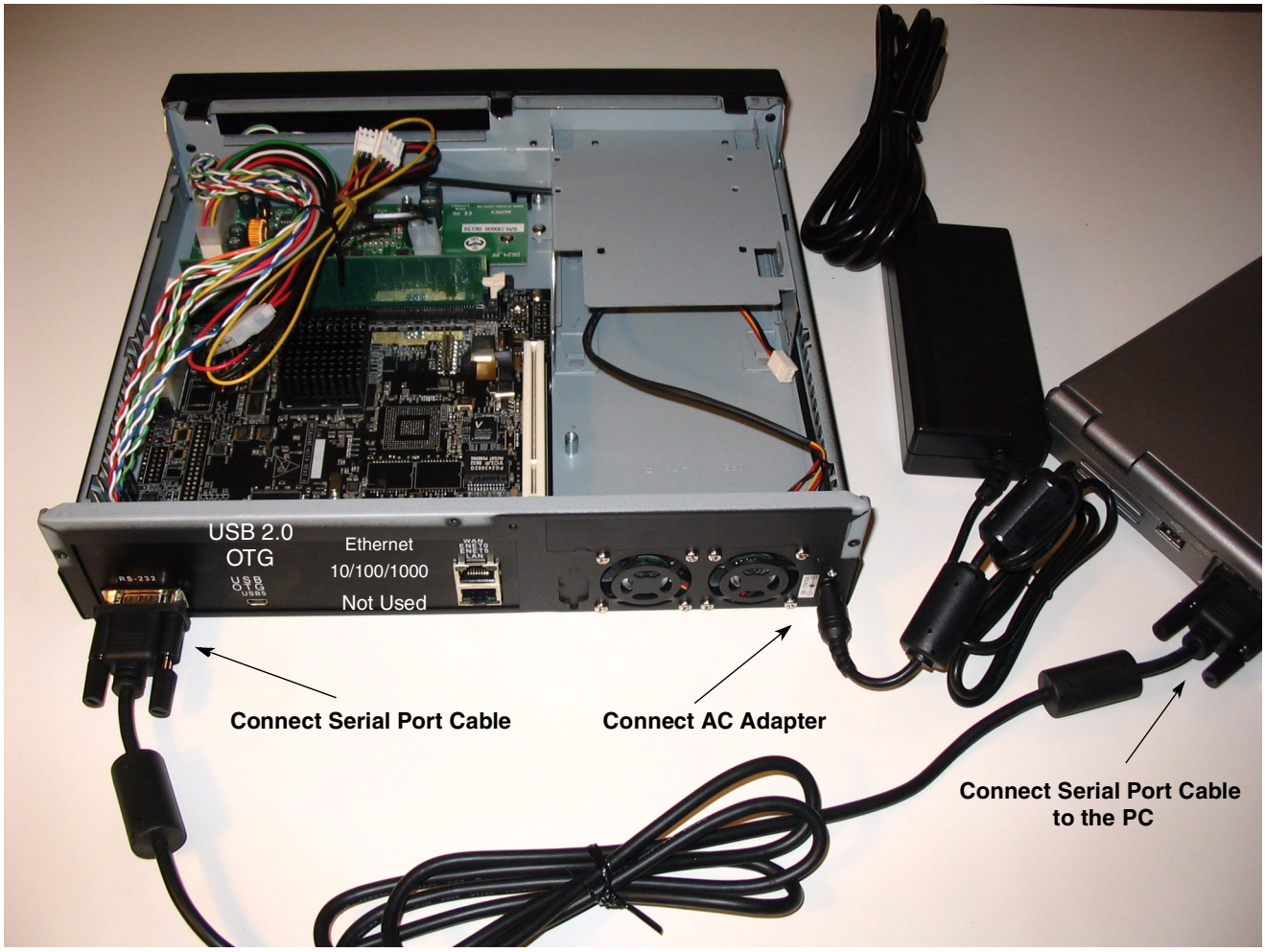

Figure 24. External Connections

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2.4 Serial Port Configuration (PC)

Before powering up the MPC8349E-mITX-GP system, configure the serial port of the attached computer as follows:

```
Data rate: 115.2 Kbps,
Number of data bits: 8,
Parity: none,
Number of Stop bits: 1,
Flow Control: Disabled.
```

2.5 Power Up

Press the power button on the front panel.

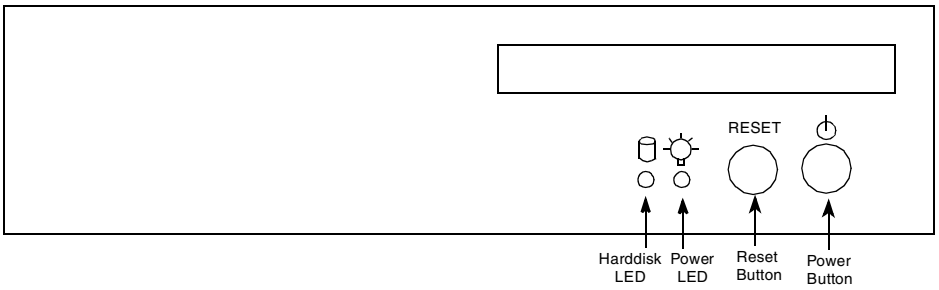

Figure 25. Front Panel

A few seconds after power up, the U-Boot prompt => should be received by the Terminal program as shown below:

```
U-Boot 1.x.x (FSL Development) (Date - time) MPC83XX


Clock configuration:
        Coherent System Bus:  xxx MHz
        Core:                 yyy MHz
        Local Bus Controller: xxx MHz
        Local Bus:             xx MHz
        DDR:                  xxx MHz
        I2C:                  xxx MHz
        TSEC1:                xxx MHz
        TSEC2:                xxx MHz
        USB MPH:              xxx MHz
        USB DR:               xxx MHz
```

…

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```
Freescale TSEC0, Freescale TSEC1

IDE:   Bus 0:

=>
```

NOTE

The normal function of the product may be disturbed by strong electromagnetic interference. If so, simply reset the product to resume normal operation by following the instruction manual. If normal function does not resume, please use the product in another location

3 MPC8349E-mITX-GP Software

A board support package (BSP) is pre-installed on the MPC8349E-mITX-GP. This BSP consists of a bootloader (u-boot), a generic PPC Linux-based system, and associated file system which reside in the on-board Flash memory. Upon power up, the Linux system is running on the MPC8349E-mITX-GP.

The MPC8349E-mITX-GP BSP generation takes advantage of a tool called the Linux Target Image Builder or LTIB. LTIB is a suite of tools that leverages existing Open Source configuration scripts and source code packages and bundles them all into a single BSP generation bundle. The source code packages include boot loaders and Linux kernel sources as well as many user-space source code packages to build a complete BSP. LTIB also provides compiler packages required to build the BSP. Freescale developers use LTIB to create BSPs for a multitude of Freescale development targets. LTIB leverages as much BSP elements as possible for all Freescale targets that are supported while offering the flexibility required to customize, as necessary, components that require platform specific modifications.

The MPC8349E-mITX-GP BSP release package contains the following:

- mpc8349e-mitx-<yyyymmdd>.iso

  This file is an ISO image that may be burned to a CD-ROM or mounted directly from your hard disk. Note that <yyyymmdd> is the release creation date.

  The LTIB installation script that installs all necessary packages on a host Linux PC and allows you to modify the BSP and packages within the BSP is in /ltib-mpc8349e-mitx subdirectory within the ISO image.

  This ISO image contains a file called Readme.txt which describes all the details required to generate and install the BSP on the MPC8349E-mITX-GP hardware platform. Readme.txt contains the latest information for each BSP release. The ISO image also contains Release Notes.txt which describes changes to the current BSP version versus earlier releases.

  To rebuild the BSP package or to add application software, follow the instructions in the Readme.txt very carefully. Readme.txt is part of the ISO release and it contains specific details on how to build, run, and install the BSP. When followed closely the Readme.txt will guide the user to achieve a successful re-installation of the BSP on the MPC8349E-mITX-GP platform.

  This ISO image contains the following documents as well:

  — MPC8349EMITXGPUG.pdf, this user's guide document in pdf format

  — MPC8349E-mITX-GP_schematic.pdf, the platform schematic in pdf format

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— SEC2SWUG.pdf: User's Guide for the Driver software of the Security engine. This document details the driver software interface of the Security Engine to boost the throughput performance of Security applications such as IPSec.

— LtibFaq.pdf, Frequently Asked Questions for LTIB, which is a useful document describing how to make use of LTIB to build the ISO image.

3.1 Third-Party Application Software

Many third-party applications are available for the MPC8349E-mITX-GP. They are typically built on top of the original BSP delivered by Freescale. To run demonstrations or to acquire details of Freescale's third-party applications for this MPC8349E-mITX-GP, contact your local Freescale sales office.

4 Revision History

Table 21 provides a revision history for this document.

Table 21. Document Revision History

Revision	Date	Substantive Change(s)
0	10/2006	Initial release. This revision of the manual corresponds to the MPC8349E-MITX-GP rev 1.0 board.

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